UDC 621.391

doi: 10.20535/2411-2976.12024.4-11

IMPLEMENTATION OF A MATCHED FILTER FOR LFM SIGNALS USING A SYSTEM-ON-CHIP BASED SDR TRANSCEIVER

Mykola M. Kaidenko, Dmytro V. Roskoshnyi

Educational and Research Institute of Telecommunication Systems
Igor Sikorsky Kyiv Polytechnic Institute, Kyiv, Ukraine

Background. Creation of communication channels with effective protection against intentional interference is the most urgent task for communication channels of unmanned aerial vehicles (UAVs). An effective solution is the use of signals with spectrum expansion, which allows reducing the impact of intentional interference on control and telemetry channels, thereby increasing the survivability of UAVs. The most optimal is the use of LCM modulation, which became possible with the development of SDR and SoC technologies. The main problem of using LFM modulation is the complexity of implementing matched filters. This requires research to create optimal digital implementations of matched filters.

Objective. The purpose of the paper is to determine the parameters of the LFM signal for the implementation of the communication system using CSS modulation on the SDR transceiver. Optimal implementation of discrete matched filter (correlator) for CSS BOK modulation on FPGA (SoC).

Methods. Analysis of the possibilities of implementing CSS BOK modulation for building a communication system based on SDR transceivers. Analysis of optimal options for building a discrete matched filter (correlator) for CSS BOK modulation on FPGA (SoC) and its implementation. Testing on a laboratory bench.

Results The possibility of creating a communication system based on an SDR transceiver using CSS BOK modulation has been confirmed. The optimal parameters of the LFM signal, which can be implemented, have been studied. An implementation of a discrete matched filter (correlator) for CSS BOK modulation on FPGA has been developed. Testing carried out on a laboratory bench using SDR transceivers AD9361 (AD9364) showed the correctness and effectiveness of the decisions made.

Conclusions The parameters of the LFM signal for the implementation in the communication system using CSS modulation on the SDR transceiver have been studied and determined. It was determined that when using the AD9361 (AD9364) transceiver, it is possible to implement an LFM signal with a band of up to 25 MHz, while the optimal symbol duration will be 16.6667 μsec at 1024 counts and a sampling frequency of 61.44 MHz. It was determined that the best CSS modulation method for creating a communication system is the binary orthogonal manipulation (BOK) method, which allows you to effectively use the advantages of SDR technologies, in particular, the ease of working with quadrature channels and, as a consequence, the ease of implementing phase synchronization. It has been determined that the best method of implementing a matched filter (correlator) on the basis of FPGA (SoC) is the application of fast convolution based on the fast Fourier transform. The developed implementation of a discrete matched filter (correlator) for CSS BOK modulation on FPGA showed the possibility of implementing a communication system with CSS BOK modulation on an SDR transceiver in full accordance with the research results. Experimental studies were carried out on a laboratory bench using SDR transceivers AD9361 (AD9364), which fully confirmed the results of simulation modelling.

Keywords: *Chirp Spread Spectrum; Matched filter; SDR; SoC; FPGA; Binary orthogonal keying; Memory-based method; UAV link.*

INTRODUCTION

Recently, more and more efforts have been paid to creating communication channels with effective protection from the effects of intentional interference. This task is most relevant for communication channels of unmanned aerial vehicles (UAVs). Intentional interference (an attack on the UAV's communication channel) can lead to irreparable consequences in the form of loss of control of the device and, as a result, the impossibility of completing the mission and the loss of the device itself.

All types of interference that can affect UAV communication channels are defined in [1]. Communication channels are the most vulnerable to energy interference, especially for small-sized UAVs due to the fact that it is not always possible to use effective methods for countering various types of interference proposed in [2]. Simple broadband interference is easily created and operates effectively in the UAV mission area, this is its harmfulness and the need to effectively counteract it.

Along with the use of methods proposed in [2] to counteract intentional interference, it is necessary to use countermeasures such as the use of spread spectrum signals, which will reduce the impact of energy interference on control and telemetry channels, increasing the survivability of the UAV. The following methods of spectrum expansion exist: Frequency Hopping Spread Spectrum (FHSS); Direct Sequence Spread Spectrum (DSSS); Chirp Spread Spectrum (CSS

© The Author(s) 2024. Published by Igor Sikorsky Kyiv Polytechnic Institute.
This is an Open Access article distributed under the terms of the license CC BY 4.0 (https://creativecommons.org/licenses/by/4.0/), which permits re-use, distribution, and reproduction in any medium, provided the original work is properly cited.

or linear frequency modulation); Time Hopping Spread Spectrum (THSS); hybrid combinations of these methods (Hybrid Spread Spectrum).

Linear frequency modulation with an extended spectrum (CSS) has been used in radar for a long time. However, the use of CSS for creation communication channels became possible only with the evolution of the elemental base of digital signal processing and the amplification of Software-Defined Radio (SDR) technologies. Software-Defined Radio combine advanced technologies to provide flexibility in radio system design by leveraging a suite of hardware and software technologies that enable most radio system functionality to be implemented in software.

The software can be modified or can be embedded, running on programmable signal processing devices: field programmable gate arrays (FPGAs), digital signal processors (DSPs), general purpose processors (GPPs), system-on-chips (SoCs) and other specialized programmable processors. Using these technologies to build SDR systems allows engineers to add new features and expand the capabilities of existing radio systems without changing the hardware platform [3].

Like other spread spectrum techniques, CSS uses the entire allocated bandwidth to transmit the signal, making it robust to channel noise. Additionally, since chirp signals use a wide spectral bandwidth, CSS is also resistant to multipath fading even when operating at very low power. However, CSS differs from FHSS and DSSS spread spectrum techniques because it does not add pseudo-random elements to the signal to help distinguish it from channel noise, instead relying on the linear nature of the chirp pulse. This difference allows for greater communication secrecy, which is especially important for UAV control channels and telemetry. Additionally, and just as importantly, CSS is resistant to the Doppler effect, which is typical for mobile communications systems. The downside of CSS is that it is difficult to implement.

I USING CHIRP SIGNALS FOR CREATION COMMUNICATION CHANNELS BASED ON SDR AND SOC TECHNOLOGIES

There are two possible methods for generating a chirp signal on an SoC (FPGA): a generator based on the use of signal samples recorded in memory (Memory-based Chirp Generator) and a generator using direct frequency synthesis (DDS) Chirp Generator [4]. Both methods have their disadvantages and advantages. Despite the worse level of signal distortion for telecommunications applications, the implementation of the Memory-based Chirp Generator option on the basis of an SDR transceiver is more acceptable due to the fact that in this way manipulation during the transition from one state (Up-Chirp) to another (Down-Chirp) is significantly simplified. and the possibility of using multi-position types of manipulation as an example of those recommended in [5] and used in LoRa technology [6].

The formation of a chirp signal in the transmitter and processing in the receiver of the SDR transceiver is carried out in the base frequency band. In addition, the use of an SDR transceiver also allows quadrature modulation, which in turn significantly simplifies signal processing in the receiver.

In general, a chirp pulse is described as:

$$s(t) = \cos(2\pi(f_0 t + \frac{\alpha}{2}t^2)) \quad (1)$$

where: $\alpha=B/T=(f1-f0)/T$; T – chirp duration.

When creating a chirp pulse in the main frequency band α=B/T=(fmax- fmin)/T, while fmax and fmin are the maximum and minimum frequencies of the pulse, respectively, regardless of how it is formed: UP-Chirp or Down-Chirp .

When representing a chirp pulse discretely, it is described as:

$$[n] = \cos(2\pi[f_0 n + \frac{\alpha}{2(N-1)}n^2]) \quad (2)$$

Using quadrature modulation allows you to imagine and create a quadrature chirp pulse, Fig. 1:

$$s[n] = \cos(2\pi[f_0 n + \frac{\alpha}{2(N-1)}n^2]) + i\sin(2\pi[f_0 n + \frac{\alpha}{2(N-1)}n^2]) \quad (3)$$

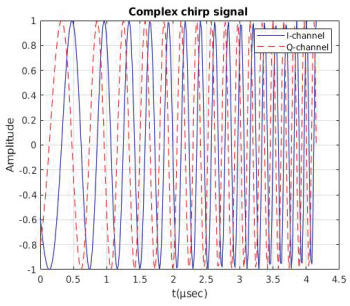


Fig. 1 - Complex representation of a discrete chirp signal

In the receiver, compression of the chirp pulse is carried out by convolving the received signal with an image, which is described in discrete representation as:

$$Y[n] = \sum_{m=0}^{n} U_m S_{(n-m)}, n = 0,...2N-1 \quad (4)$$

where: $Y[n]$ - samples of the convolution result;

U_m - samples of the input signal;

$S_{(n-m)}$ - samples of the chirp reference signal

Direct implementation of convolution according to (4) is an expensive operation, since its calculation requires O(N2) operations. To reduce the number of operations, a more optimal version of fast convolution using FFT is used, which requires an order of O(Nlog(N)) operations:

$$Y = IFFT(FFT(U) * FFT(S^*)) \quad (5)$$

where: S^* - complex conjugate chirp reference signal

Fig. 2 shows an implementation of convolution using FFT. It is worth noting that fast convolution using FFT stasis implies a robot with a complex representation of the signal, which is very useful when using quadrature modulation in an SDR transceiver and a complex representation of the chirp signal. The complex representation of the chirp has another important advantage when processing in the receiver - when the signal is discretely represented and convolution is used to obtain the correlation function, synchronization of the initial phase of the pulse is not required.

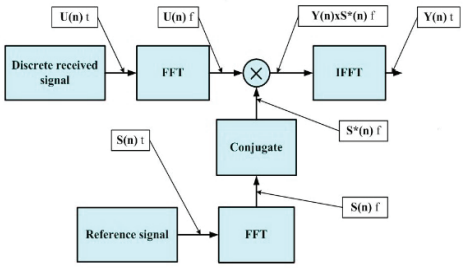


Fig. 2 – Implementation of convolution using FFT

Chirp spread spectrum systems can be divided into two categories: binary orthogonal keying (BOK) and direct modulation (DM). The BOK CSS system uses two different chirps with the same bandwidth and duration, but with opposite sweep polarity - UP-Chirp and Down-Chirp. The block diagram of the BOK CSS system is shown in Fig. 3. Here, UP-Chirp and Down-Chirp are used to represent different data symbols: bits "1" and "0" are represented by pulses with positive and negative instantaneous rate of change of frequency, respectively. At the receiver side, appropriate matched filters are used to decode the received signal.

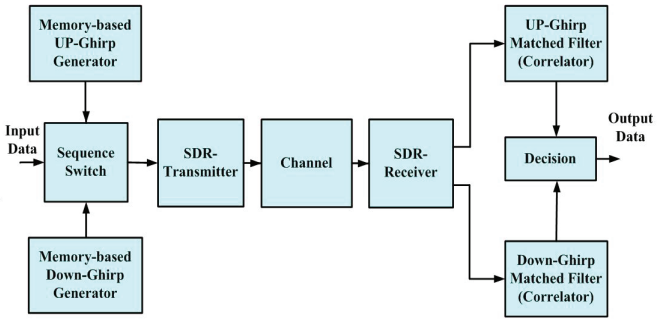


Fig.3 - Implementation principle BOK CSS system

The DM CSS system uses pulsed signals as a timing mechanism rather than as signalling. This system is similar in concept to DSSS systems. Similar to the pseudo noise (PN) sequence in DSSS systems, the chirp signal performs a similar function in the DM CSS system [7].

In DM CSS systems, chirps are used only for the purpose of expansion and compression, while the data is modulated using the usual incoherent modulation scheme. Consequently, the CSS DM system is more difficult to implement than the CSS BOK system. The DM method must be combined with other digital modulation schemes for data transmission, but the BOK method is not. Thus, the modulation scheme of the BOK method for wireless data transmission is simpler than the modulation scheme of the DM method. Moreover, the BOK chirp method uses two different signals for data modulation, while the DM chirp method can only use one chirp signal for expansion.

Therefore, the DM method focuses on the autocorrelation of the LFM signal, which is the same as in the radar system, while the BOK method depends not only on the characteristics of the autocorrelation, but also on the characteristics of the mutual correlation between the two selected LFM signals, Fig. 4, which makes it is more resistant to interference when the communication channel is exposed to intentional interference. The BOK method is more suitable for chirp analysis, since its performance depends more on the chirp characteristics than the DM method. Fig. 4 shows the result of the ACF and CCF modelling for a sequence with the following parameters: length 1024 points, chirp duration 16.6667 μsec, chirp bandwidth 25 MHz (1 MHz - 26 MHz)

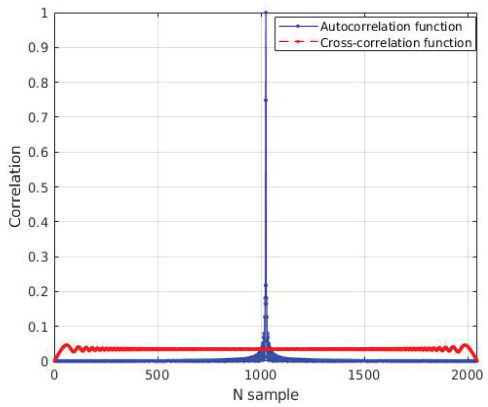


Fig. 4 - Characteristics of auto- and cross-correlation between Ur-Chirp and Down-Chirp

II IMPLEMENTATION OF THE SOC-BASED MATCHED FILTER

Matched filtering is the process of detecting a known signal distorted by noise, i.e. a correlation operation is performed between the received signal and its known image. At the output of the matched filter, we get a compressed signal, that is, the matched filter is used as a pulse compression filter, which provides a high signal-to-noise ratio at its output. The impulse response of the matched filter is a time-reversed and conjugate image copy of the transmitted signal.

One of the options for building matched filters is the implementation of convolution using the forward (FFT) and inverse Fourier transform (IFFT). [8,9] In this case, the Fourier transformation is performed on the signal and its image (transition from time to frequency form), after that, Fourier-image multiplication and the inverse Fourier transformation (transition from frequency to time form) are performed. of this product. After this procedure, in the presence of a received mixture of signal and noise, we get a short compressed pulse [10]. A simplified diagram of such a matched filter is shown in Fig. 2.

When implementing a matched filter in the SoC based on the scheme shown in Fig. 2, it is necessary to generate a reference LFM signal

Two ways of digital implementation of the solution to this problem are possible. The first one is based on the use of memory, and the second one is a direct digital synthesis of DDS [4,11].

The implementation based on the Memory-based method is based on the fact that all readings of the LFM signal are recorded in the FPGA memory and read from it with the required clock frequency. Reading management is reduced to the formation with the help of a counter of the address on which the necessary data is located.

The method of direct digital synthesis also implies the use of a memory in which the readings of one period of the sinusoid are stored, on the basis of which the LFM signal is formed. The reading control in this case is carried out with the help of a phase accumulator, which is a combination of a counter and an accumulator.

Using the symmetry properties of the sinusoid allows you to reduce the required amount of memory, but at the same time, the algorithm and the structure of the reading control are significantly complicated.

Thus, the formation of the reference LFM signal using the Memory-based method is more preferable, since the read control system is simpler compared to DDS and requires less resources in the implementation on the FPGA

The matched filter, built according to the scheme shown in Fig. 2, uses one reference signal, and in this form is most often used in radar applications. At the same time, the main task is to detect and determine the delay of the received echo signal

For use in BOK CSS systems, this scheme must be modified. Up-Chirp and Down-Chirp reference signals are formed using the Memory-based method using dual-port memory. The use of dual-port memory allows simultaneous access to its contents located at different addresses.

Not only the values of the complex readings of the reference signals, but also the results of the Fourier transformation over them can be recorded in the memory. FFT implementation requires a significant number of multiple and, as a result, hardware DSP-blocks, the number of which is limited. Therefore, such a solution allows you to reduce hardware costs when implementing this algorithm in the FPGA part of the SoC, since there is no need to conduct FFT over the reference signals.

Another advantage of this solution is the ability to work with complex signals.

The reading control scheme in this case consists of two synchronous counters - up-counter and down-counter. Both counters have the same calculation module. Such a solution allows you to synchronously generate Up-Chirp and Down-Chirp reference signals. Further processing is carried out in accordance with the algorithm of Fig. 5

In order to experimentally confirm the results obtained during theoretical studies, a laboratory stand was assembled, consisting of a transmitter of a stream of LFM pulses, a receiver of a stream of LFM pulses, and tools for visualizing the obtained results.

The ADALM-Pluto module, Fig. 6, was used as a transmitter of the sequence of LFM pulses [12]. The

flow of LFM pulses during testing was a cyclic transmission of the Up-Chirp/Down Chirp sequence with a length of 20 pulses. based on the module

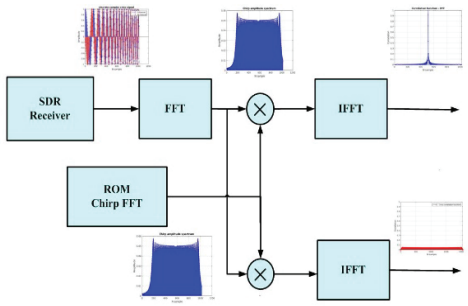


Fig.5 - Memory-based Implementation BOK CSS system

The module is used in the DAC Buffer Output mode for the sampling frequency f sample = 61.44 MHz. RF Bandwidth = 56 MHz, carrier frequency = 2400 MHz.

Fig. 6 - Transmitter of the sequence of LFM pulses based on the ADALM-Pluto module

The DE-10 Standard board based on the SoC Cyclone V SX—5CSXFC6D6F31C6 with the Arradio SDR transceiver, installed on it, was used as the receiver [13], [14], Fig. 7. Sampling frequency = 61.44 MHz. RF Bandwidth = 56 MHz. Display of the transmitter settings mode and the received signal was carried out using the ADI IIO Oscilloscope

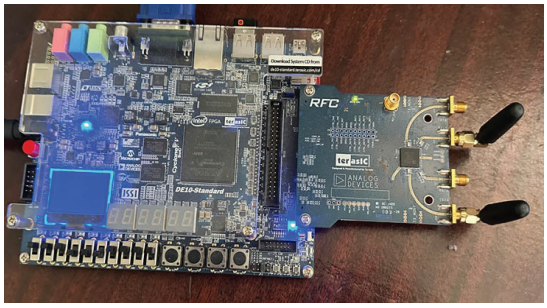


Fig. 7 – Receiver of the sequence of LFM pulses

The matched filter of the LFM signal flow receiver is implemented on the basis of Intel SoC Cyclone V SX—5CSXFC6D6F31C6 using the Quartus Prime package. The use of this particular package is due to the authors having significant prior experience in SoC development using devices and development tools from Intel (Altera). Modules created in the Verilog language and IR cores from the Quartus Prime package were used to build the matched filter.

Chirp parameters used for modelling and experimental studies are listed in Table 1

Table 1 – Chirp parameters used for modelling and experimental studies

Parameter	Value
Sampling frequency (ADC)	491.52 MHz
Sampling frequency (SoC input)	61.44 MHz
Chirp duration	16.6667 µsec
Chirp bandwidth	25 MHz (1 MHz - 26 MHz)
Chirp slope	1.5 MHz/µsec
Data format	12 bit
Total sample points	1024

Fig. 8 shows a photo of the test bench, the DE-10 Standard monitor displays the received signal in the time domain

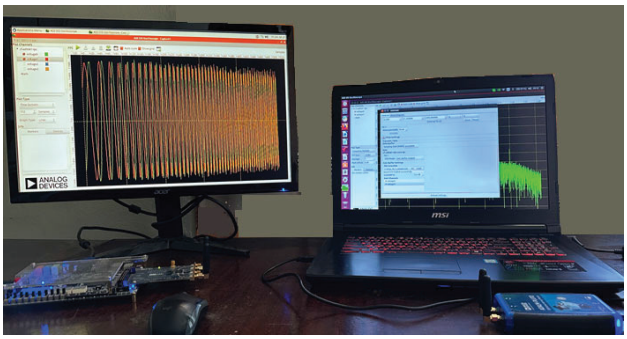


Fig. 8 – The received signal in the time domain on the DE-10 Standard monitor

The calculated spectrum of a single LFM pulse is shown in Fig. 9. Fig. 10 shows a photo of the test bench, the spectrum of the received signal is displayed on the DE-10 Standard monitor

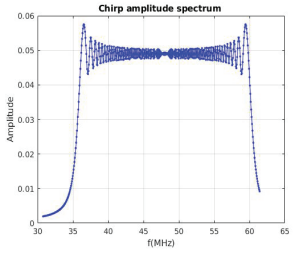


Fig. 9 – The calculated spectrum of a single LFM pulse

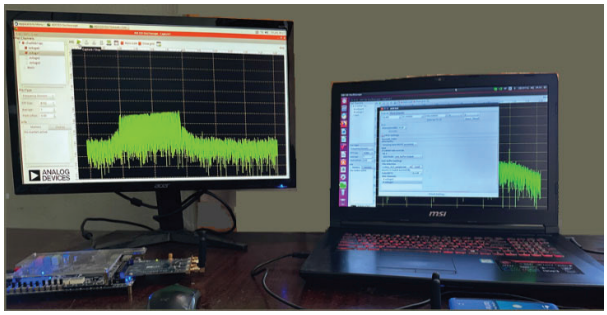
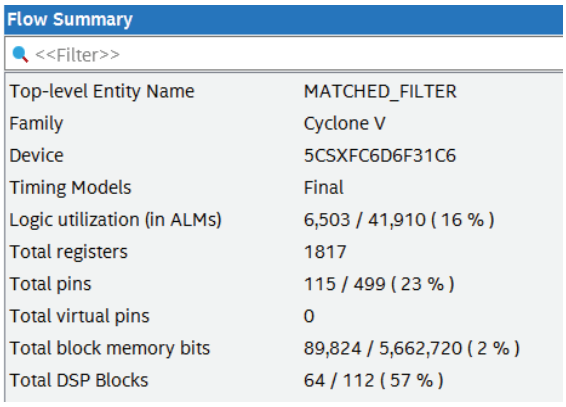


Fig. 10 – Spectrum of the received sequence of LFM pulses on the DE-10 Standard monitor

The parameters of the implementation of the matched filter based on SoC Cyclone V SX are shown in Table 2, and the results of the physical implementation of the matched filter in the Quartus Prime environment are shown in Fig. 11.

Table 2 – Implementation parameters of the matched filter

Parameter	Value
FFT/IFFT length	1024
Sampling frequency (SoC input)	61.44 MHz
Chirp duration	16.6667 µsec
Chirp bandwidth	25 MHz (1 MHz - 26 MHz)
Chirp slope	1.5 MHz/µsec
Input data format	12 bit
Logic utilization (in ALMs)	6.503/41.910 (16 %)
Total block memory bits	89.824/5.662.720 (2%)
Total DSP Blocks	64/112 (57 %)



Flow Summary	
<<Filter>>	
Top-level Entity Name	MATCHED_FILTER
Family	Cyclone V
Device	5CSXFC6D6F31C6
Timing Models	Final
Logic utilization (in ALMs)	6,503 / 41,910 (16 %)
Total registers	1817
Total pins	115 / 499 (23 %)
Total virtual pins	0
Total block memory bits	89,824 / 5,662,720 (2 %)
Total DSP Blocks	64 / 112 (57 %)

Fig. 11 – Results of the physical implementation of the matched filter in the Quartus Prime environment for SoC Cyclone V SX

The results of the physical implementation of the matched filter shows that the most critical resource is DSP Blocks, which are mainly used to perform Fourier transformation. At the same time, logic utilization and memory utilization are quite low.

III CONCLUSIONS

This article analyses the possibilities and advantages of using chirp signals in telecommunications applications, in particular in UAV telemetry and control channels. Today's level of microelectronics development makes it possible to widely use advanced SDR technologies to create SoC-based transceivers.

One of the key elements of processing a received chirp signal is a matched filter, in which the operation of correlating the received signal and the transmitted one is performed.

It was determined that the best CSS modulation method for creating a communication system is the binary orthogonal manipulation (BOK) method, which allows you to effectively use the advantages of SDR technologies, in particular, the ease of working with quadrature channels and, as a consequence, the ease of implementing phase synchronization.

It was determined that the best method of implementing a matched filter (collerator) on the basis of FPGA (SoC) is the application of fast convolution based on the fast Fourier transform. In this case, the receiver must have copies of both reference signals. In the proposed implementation of a matched filter, reference signals are generated based on the Memory-based method.

In the proposed implementation of a matched filter, the correlation function is simultaneously calculated for both reference signals. This allows you to make an unambiguous decision due to the low cross-correlation between them.

It was established that when using the AD9361 (AD9364) transceiver, it is possible to implement an LFM signal with a band of up to 25 MHz, while the optimal symbol duration will be 16.6667 µsec at 1024 counts and a sampling frequency of 61.44 MHz.

The developed FPGA implementation of a discrete matched filter (correlator) for CSS BOK modulation showed the possibility of implementing a communication system with CSS BOK modulation on an SDR transceiver in full accordance with the research results. Experimental studies were carried out on a laboratory bench using SDR transceivers AD9361 (AD9364), which fully confirmed the results of simulation modelling.

References

1. Mykola M. Kaidenko, Serhii O. Kravchuk “PROTECTION AGAINST THE EFFECT OF DIFFERENT CLASSES OF ATTACKS ON UAV CONTROL CHANNELS” Information and

Telecommunication Sciences, No.1, pp. 35-43, 2022. https://doi.org/10.20535/2411-2976.12022.35-43
2. Kaidenko M., Kravchuk S. (2021) Autonomous Unmanned Aerial Vehicles Communications on the Base of Software-Defined Radio. In: Ilchenko M., Uryvsky L., Globa L. (eds) Advances in Information and Communication Technology and Systems. MCT 2019. Lecture Notes in Networks and Systems, vol 152. Springer, Cham. https://doi.org/10.1007/978-3-030-58359-0_16
3. M.M. Kaidenko, D.V. Roskoshnyi, Software Defined Radio in Communications. In: Advances in Information and Communication Technologies, M. Ilchenko, L. Uryvsky, L. Globa (eds), UKRMICO 2018. Lecture Notes in Electrical Engineering, vol 560. Springer, Cham (2019), https://doi.org/10.1007/978-3-030-16770-7_11 (Print ISBN 978-3-030-16769-1).
4. Chua Ming Yam, and Voon Koo, "FPGA-Based Chirp Generator for High Resolution UAV SAR," *Progress In Electromagnetics Research*, Vol. 99, 71-88, 2009.doi:10.2528/PIER09100301
5. "IEEE Standard for Low-Rate Wireless Networks," in *IEEE Std 802.15.4-2020 (Revision of IEEE Std 802.15.4-2015)* , vol., no., pp.1-800, 23 July 2020, doi: 10.1109/IEEESTD.2020.9144691.
6. Noor-A-Rahim, M.; Khyam, M.O.; Mahmud, A.; Li, X.; Pesch, D.; Poor, H.V. Hybrid Chirp Signal Design for Improved Long-Range (LoRa) Communications. *Signals* 2022, *3*, 1-10. https://doi.org/10.3390/signals3010001
7. J. Pinkney and A. Sesay, "Performance of N-ary chirp spread spectrum modulation in the AWGN and broadband multipath channels," presented at the 2004 Wireless proceedings, Calgary, Alberta, 2004.
8. L. Brigham, “The fast Fourier transform and its applications”, Prentice Hall, 1988
9. R.G. Lyons, “Understanding digital signal processing”, Prentice Hall, 4th edition, 2010
10. Sameh G. Salem, “Enhancement of Matched Filter Response for Chirp Radar Signals using Signal Recovery Technique”, International Journal of Innovative Technology and Exploring Engineering (IJITEE),ISSN: 2278-3075 (Online), Volume-9 Issue-2, December 2019
11. H. Yang, S. -B. Ryu, H. -C. Lee, S. -G. Lee, S. -S. Yong and J. -H. Kim, "Implementation of DDS chirp signal generator on FPGA," *2014 International Conference on Information and Communication Technology Convergence (ICTC)*, Busan, Korea (South), 2014, pp. 956-959, doi: 10.1109/ICTC.2014.6983343
12. Adalm-Pluto [Online]. Retrieved from: https: //www.analog.com/en/resources/evaluation-hardware-and-software/evaluation-boards-kits/adalm-pluto.html#eb-overview Accessed on: May 13, 2024.
13. DE10-Standard [Online]. Retrieved from: https://www. terasic.com.tw/cgi-bin/page/archive.pl?Language =English&No=1081 Accessed on: May 13, 2024.
14. HSMC ARRadio Daughter Card [Online]. Retrieved from: https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=65&No=946 Accessed on: May 13, 2024.

Кайденко М.М., Роскошний Д.В.

Реалізація узгодженого фільтру для ЛЧМ сигналів при використанні SDR трансивера на базі System-on-Chip

Проблематика. Створення каналів зв'язку з ефективним захистом від впливу на них навмисних перешкод є найбільш актуальним завданням для каналів зв'язку безпілотних літальних апаратів (БПЛА). Ефективним рішенням є використання сигналів з розширенням спектру, що дозволяє зменшити вплив навмисних завад на канали управління і телеметрії, повищуючи тим самим живучість БПЛА. Найбільш оптимальним є використання ЛЧМ модуляції, яке стало можливим з розвитком SDR та SoC технологій. Основна проблема застосування ЛЧМ модуляції полягає в складності реалізації узгоджених фільтрів. Це вимагає проведення досліджень по створенню оптимальних цифрових реалізації узгоджених фільтрів.

Мета досліджень. Визначення параметрів ЛЧМ сигналу для реалізації системи зв’язку з використанням CSS модуляції на SDR трансивері. Оптимальна реалізація дискретного узгодженого фільтру (корелятора) для CSS BOK модуляції на FPGA (SoC).

Методика реалізації. Аналіз можливостей реалізації CSS BOK модуляції для побудови системи зв’язку на базі SDR трансиверів. Аналіз оптимальних варіантів побудови дискретного узгодженого фільтру (корелятора) для CSS BOK модуляції на FPGA (SoC) та його реалізація. Тестування на лабораторному стенді.

Результати досліджень. Підтверджено можливість створення системи зв’язку на базі SDR трансивера з використанням CSS BOK модуляції. Досліджено оптимальні параметри ЛЧМ сигналу, які можуть бути реалізовані. Розроблено реалізацію дискретного узгодженого фільтру (корелятора) для CSS BOK модуляції на FPGA. Проведене тестування на лабораторному стенді з використанням SDR трансиверів AD9361 (AD9364) показало правильність та ефективність прийнятих рішень.

Висновки. Досліджено та визначено параметри ЛЧМ сигналу для реалізації системи зв'язку з використанням CSS модуляції на SDR трансивері. Визначено, що при використанні трансивера AD9361 (AD9364) можна реалізувати ЛЧМ сигнал смугою до 25 МГц, при цьому оптимальна тривалість символу складатиме 16.6667 μsec при 1024 відліках та частоті дискретизації 61,44 МГц. Визначено, що найкращим методом CSS модуляції для створення системи зв'язку є метод бінарної ортогональної маніпуляції (BOK), який дозволяє ефективно використовувати переваги SDR технологій, зокрема простоту роботи з квадратурними каналами і як наслідок простоту реалізації фазової синхронізації. Визначено, що найкращим методом реалізації узгодженого фільтру (корелятора) на базі FPGA (SoC) є застосування швидкої згортки на базі швидкого перетворення Фур'є. Розроблена реалізація дискретного узгодженого фільтру (корелятора) для CSS BOK модуляції на FPGA показала можливість реалізації системи зв'язку з CSS BOK модуляцією на SDR трансивері у повній відповідності з результатами досліджень. Проведено експериментальні дослідження на лабораторному стенді з використанням SDR трансиверів AD9361 (AD9364), які повністю підтвердили результати імітаційного моделювання.

***Ключові слова**: ЛЧМ модуляція; узгоджений фільтр; SDR; SoC; FPGA; двійкова ортогональна маніпуляція; Memory-based method; канал зв'язку БПЛА.*